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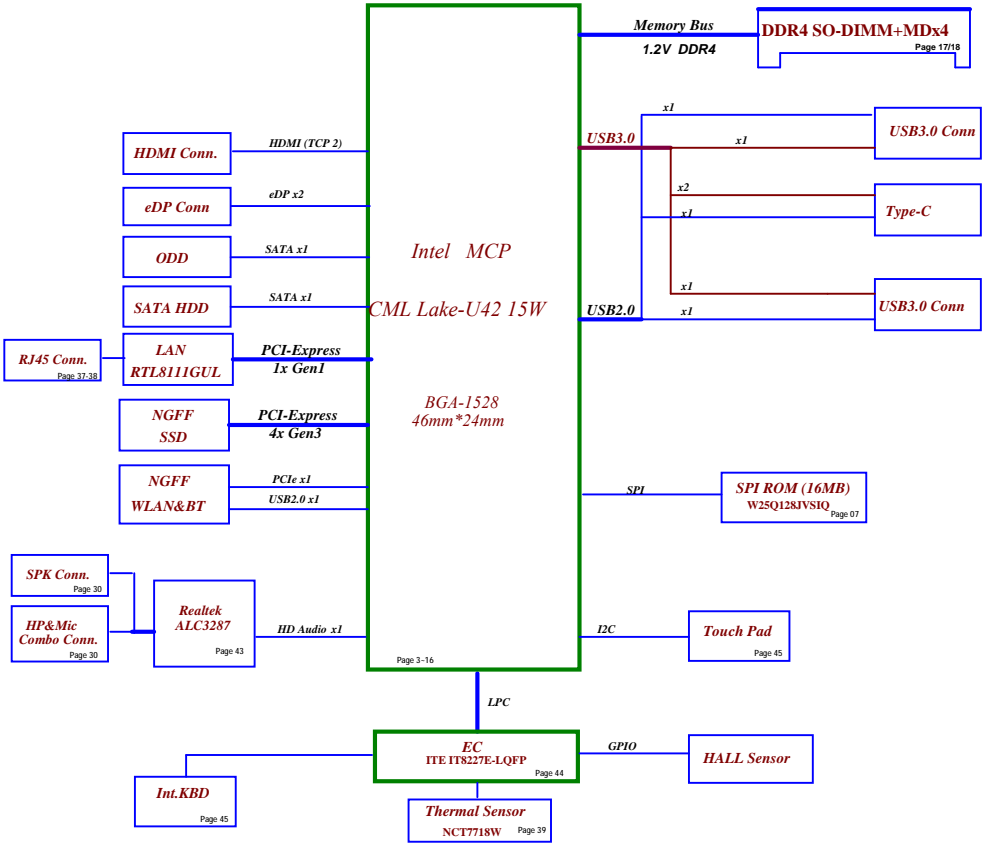
HG560 MB Schematics Document

ITL UP3 with DDR4

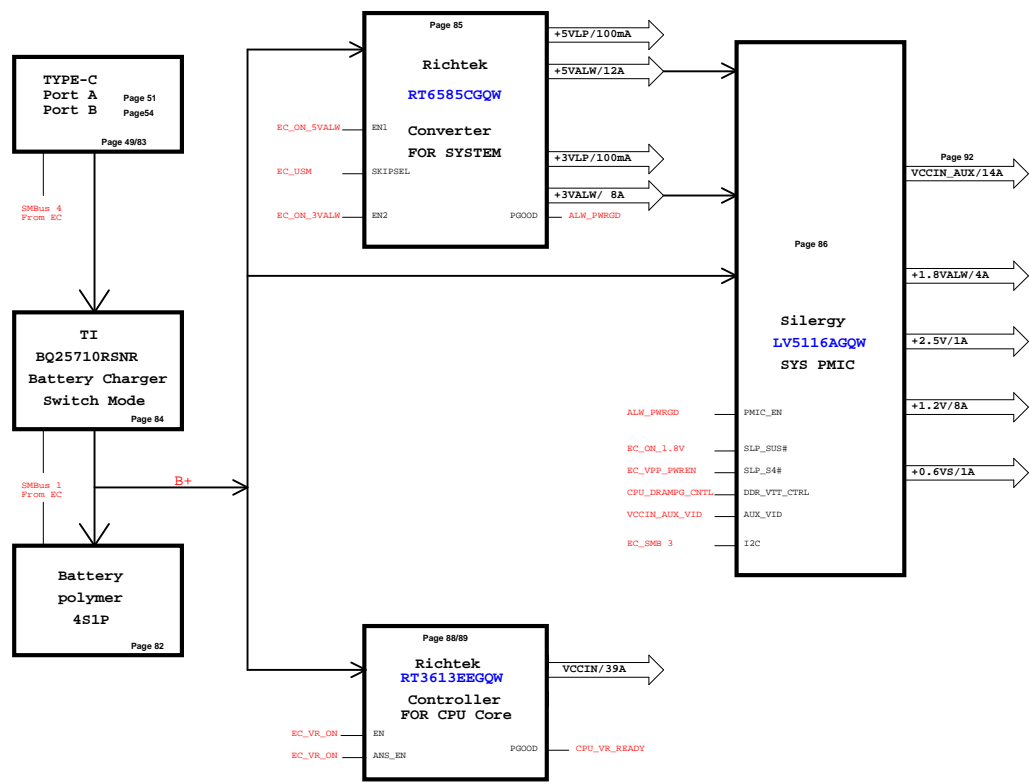
2020-06

REV: 0.1

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			Rev	0.1	
			Date	Wednesday, August 11, 2020 1:59 PM	



Block Diagram_Power



Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+SVS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
State				
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

[illegible]

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Right
	2	USB3.0 Conn Left
	3	NC
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	NC
	3	USB3.0 Conn Right
	4	Finger Print
	5	Card reader
	6	NC
	7	Camera
	8	NC
	9	NC
	10	Bluetooth
PCI-E	5-8 X4	DGPU
	9	Giga LAN
	10	NC
	11	SATA HDD
	12	WLAN
	13-16 X4	PCI-E/SATA SSD


BOM Structure	ATO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
YOGA@	For YOGA530 part
530@	For 530s part
CD@	For C cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_N@	For EMC un-stuff part
EMC_PX@	For EMC PX part
EMC_PXN@	For EMC PX nu-stuff part
NB@	For NB part
OPT@	For NV GPU part
OPTN16@	For NV N16-OTR GPU part
OPTN17@	For NV N17-G1 GPU part
T\$@	For touch screen part
TP@	For Touch Pad Part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCI	PMIC	SODIMM	Thermal Sensor	WLAN
BC_SMB_CLK1 BC_SMB_DA1	IT8586E +3VL_BC	V	V	X	V +3VL_BC	X	X	X	X	X	X
BC_SMB_CLK2 BC_SMB_DA2	IT8586E +3VS	X	X	V +3VL_AGN	V +3VS	X	V +3VALN_PCH	X	X	V	X
BC_SMB_CLK3 BC_SMB_DA3	IT8586E +3VL_BC	X	X	X	V +3VL_BC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALN_PCH	X	X	X	X	X	V +3VALN_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address	EC SMBus2 address	EC SMBus3 address	PCH SM Bus address
0x48	0x48	0x48	0x48

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100ab	PMC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	PCH	need to update			Wlan	Reserved
		DGPU	need to update				

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P05-Notes For VGA

Version: 1.0 Date: 2009-12-15

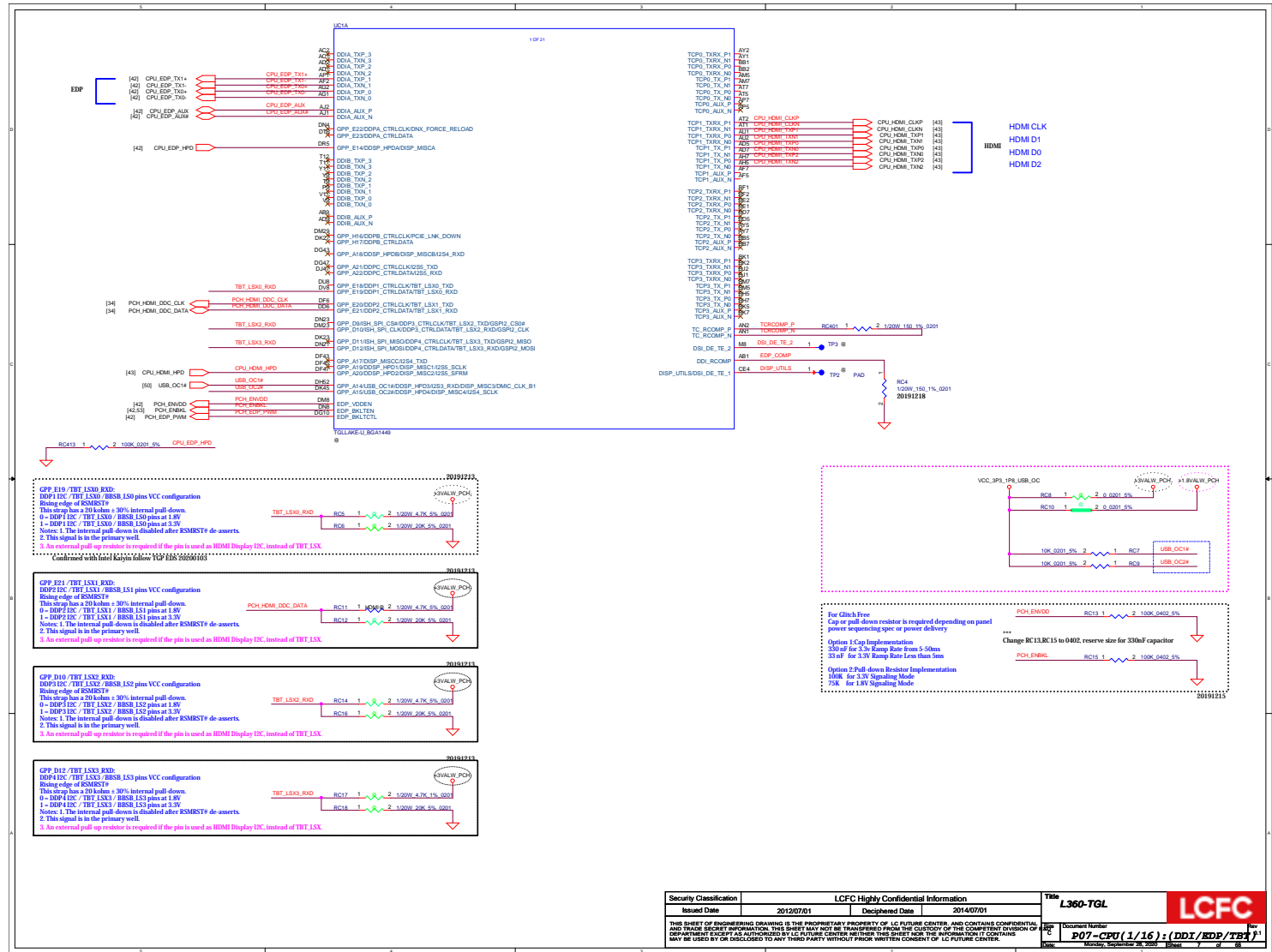
Virtual Symbol_Power

PCB	
CPU	
GPU	
DRAM MD	
VRAM	
X76	
DRAM SODIM	
Re-Timer	

15W	25W

[illegible]

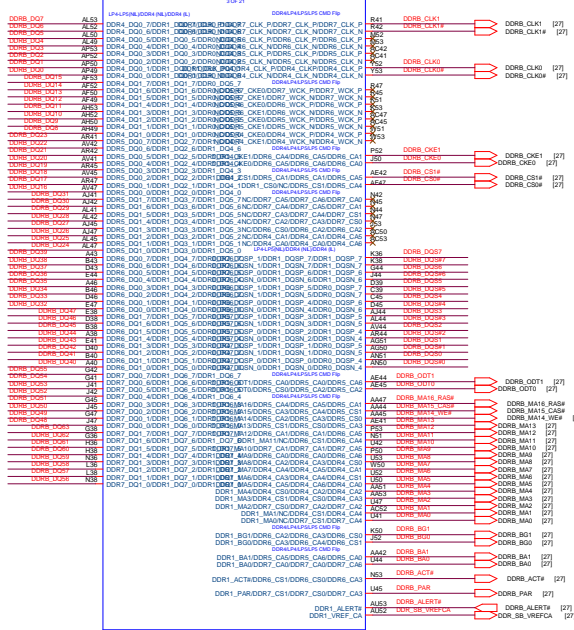
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[27] DOR8_DQ[0:63]  DOR8_DQ[0:63]

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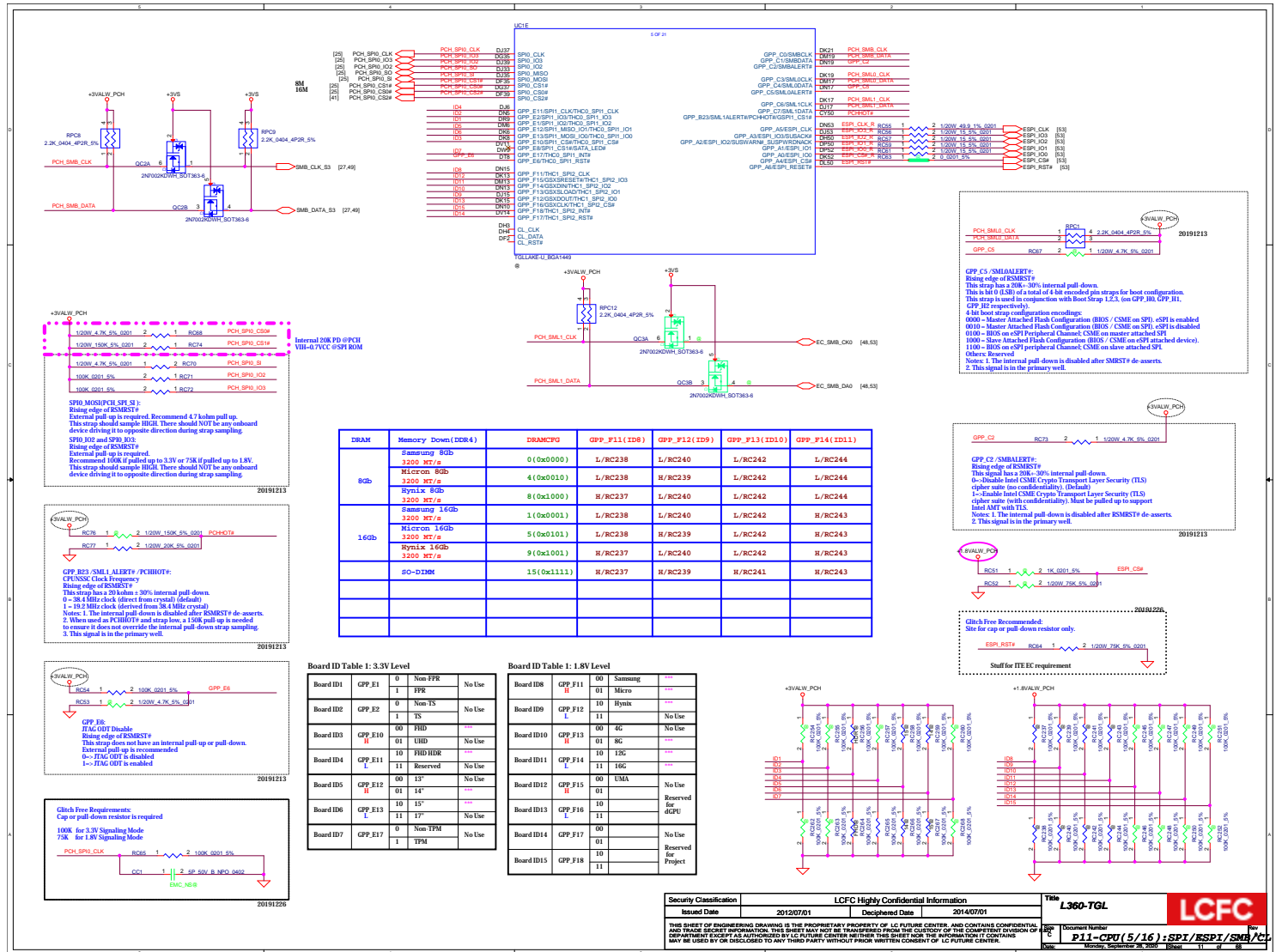
3 OF 21

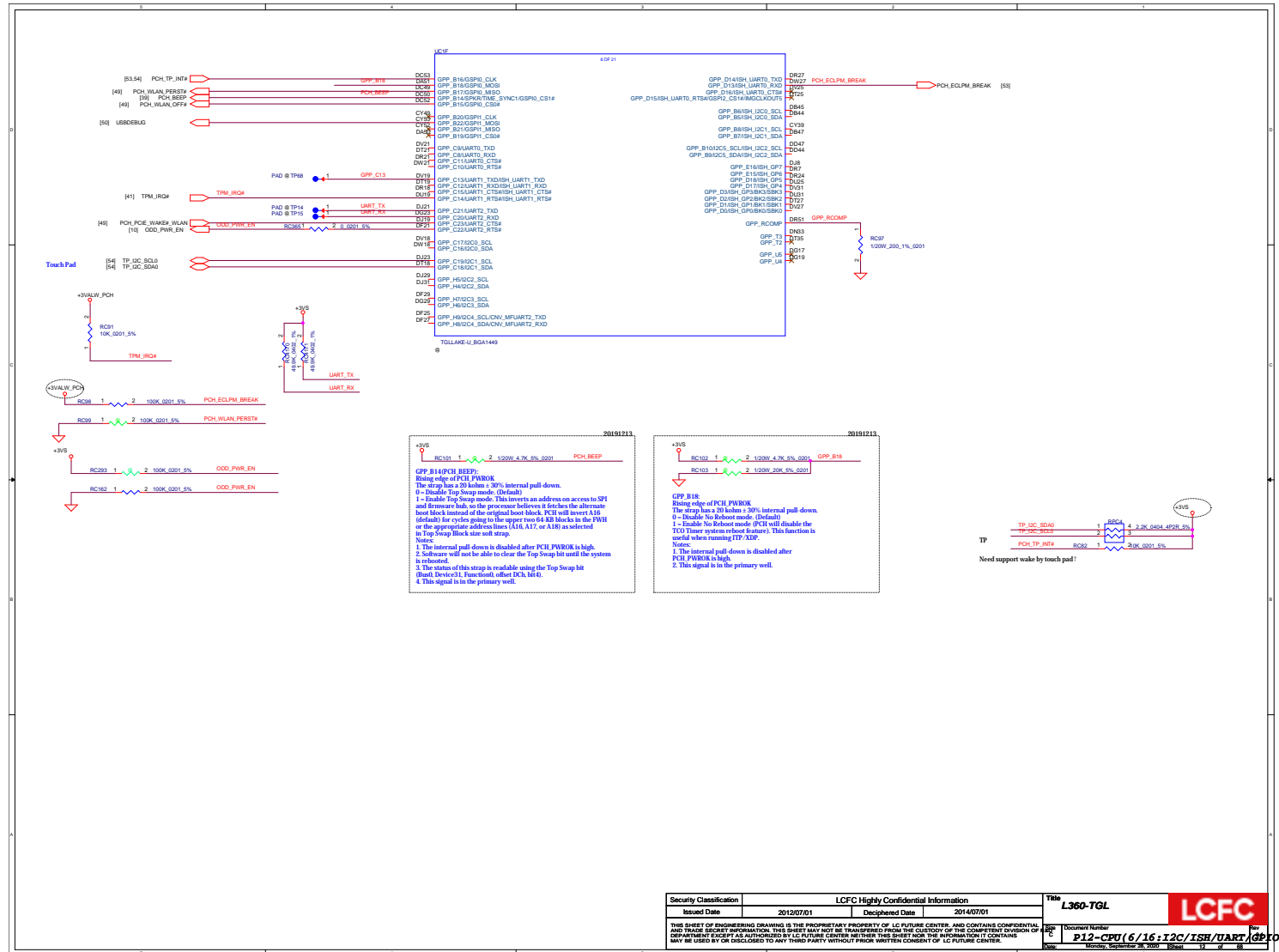


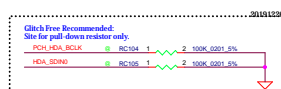
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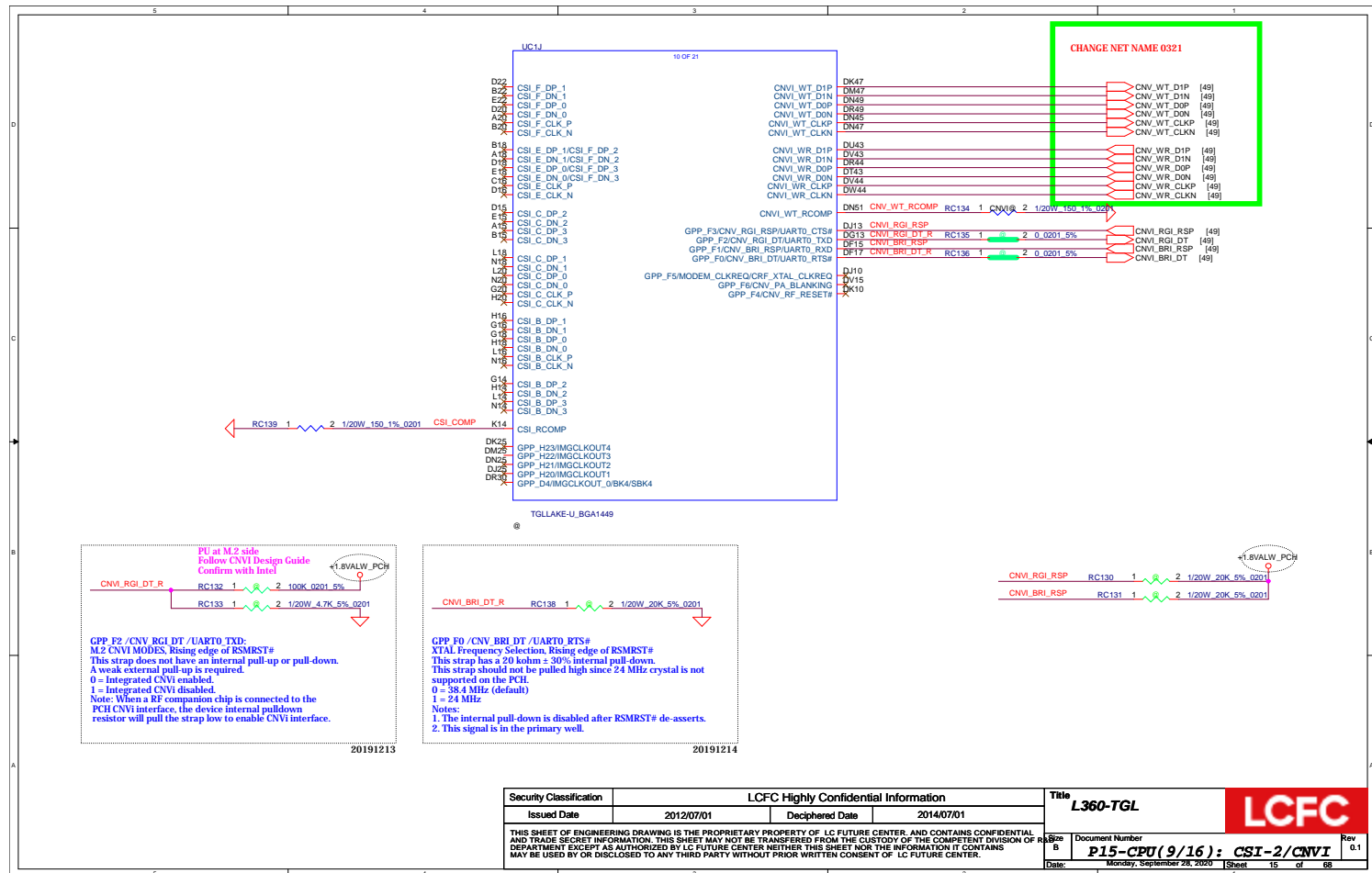
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Doc No.	P09-CPU(3/16): (DDR4-Chane) JB			Version	2014.11.200
				Page	9 of 88

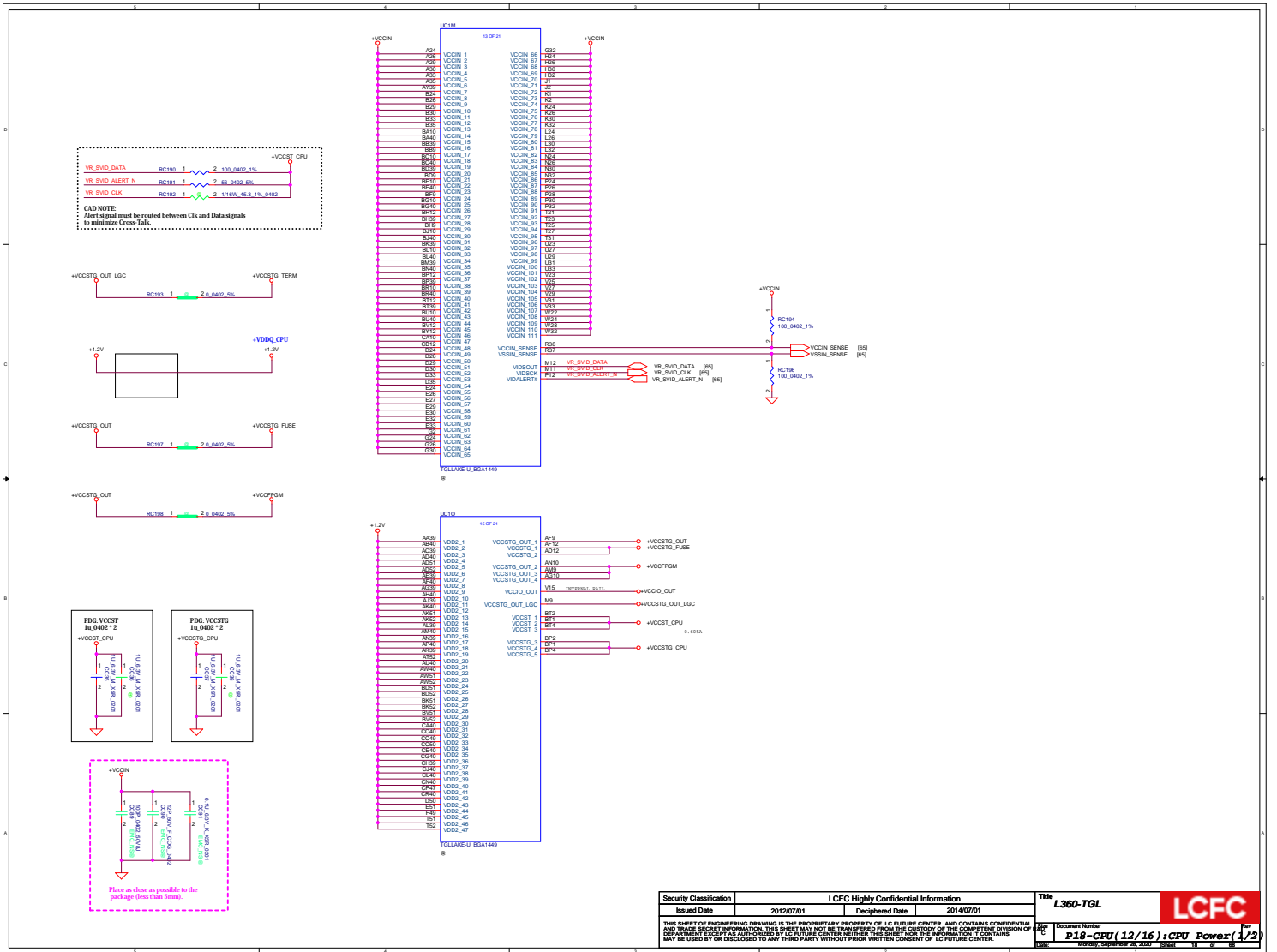




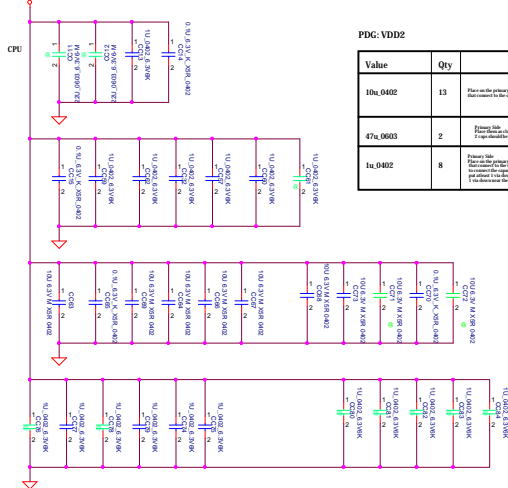


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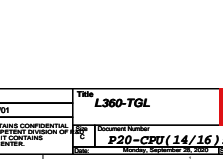
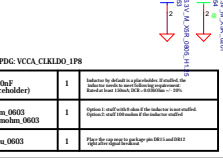
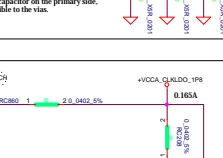
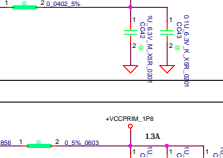
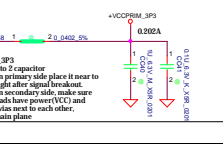
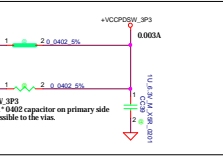
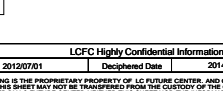
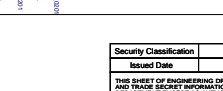
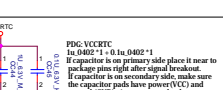
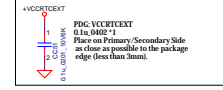
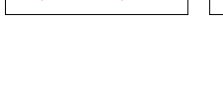
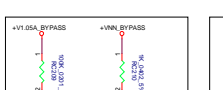
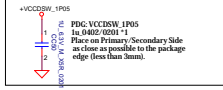
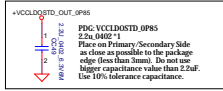
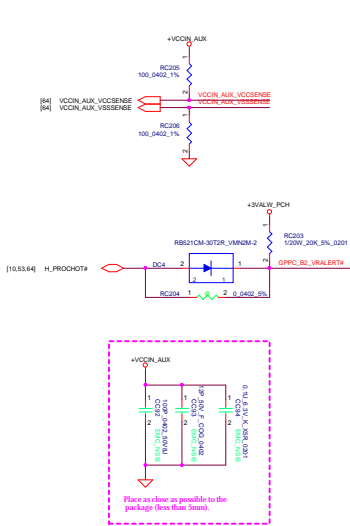
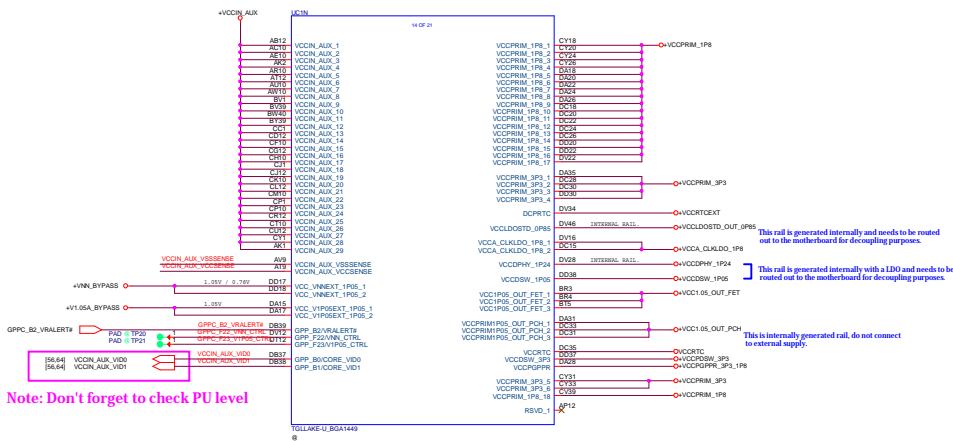
VDD2
+1.2V PDG: 2*47UF+ 13*10UF+8*1UF

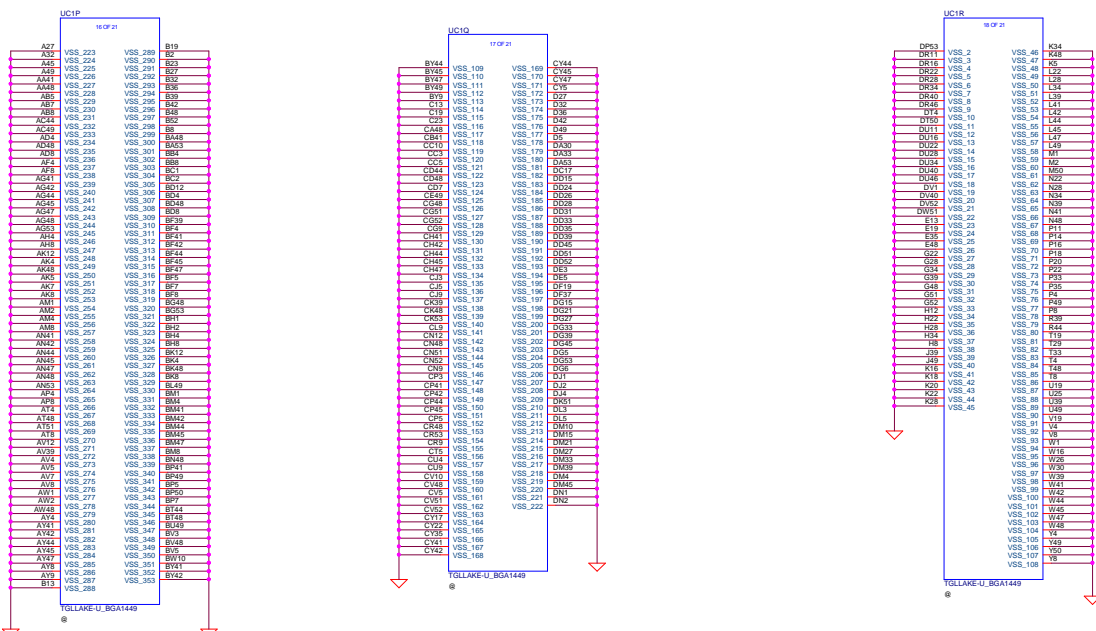


PDG: VDD2

Value	Qty	Note
10u,0402	13	Place on the primary side, as close as possible to the chip that connects to the power plane of the chip
47u,0603	2	Primary side 2* 47uF capacitors on the 1.2V as possible
1u,0402	8	Primary side 8* 1uF capacitors on the 1.2V as possible to the chip that connects to the power plane of the chip. The capacitors should be placed on the secondary side of the chip, as close as possible to the chip. The capacitors should be placed on the secondary side of the chip, as close as possible to the chip. The capacitors should be placed on the secondary side of the chip, as close as possible to the chip.

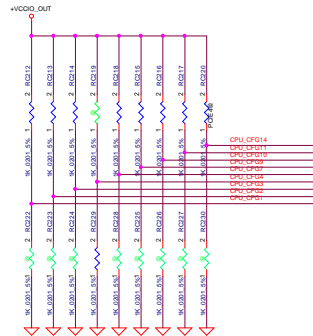
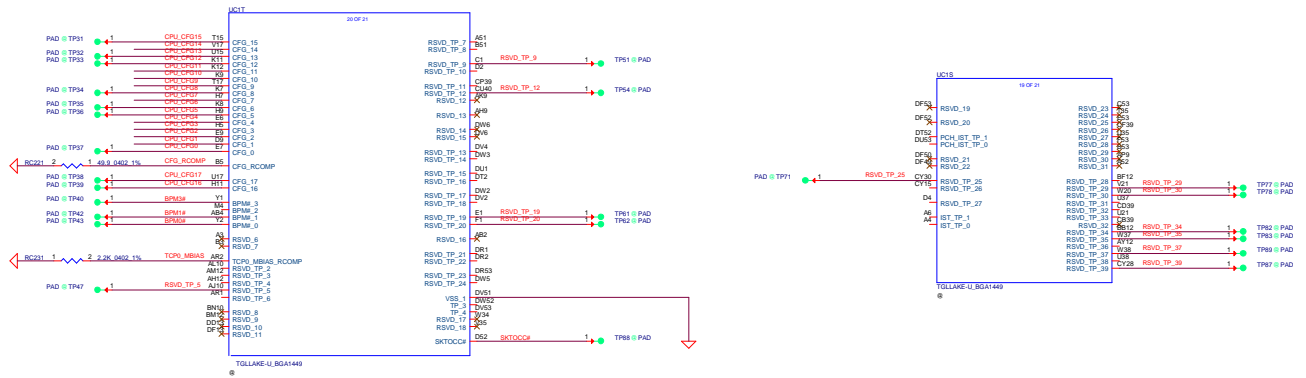
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	P19-CPU (13/16) : CPU Power					2/2
	Version: 1.0					





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Confirm		P21-CPU(15/16) : QND		0.1	
Date		Wednesday, August 13, 2015		Sheet 21 of 58	

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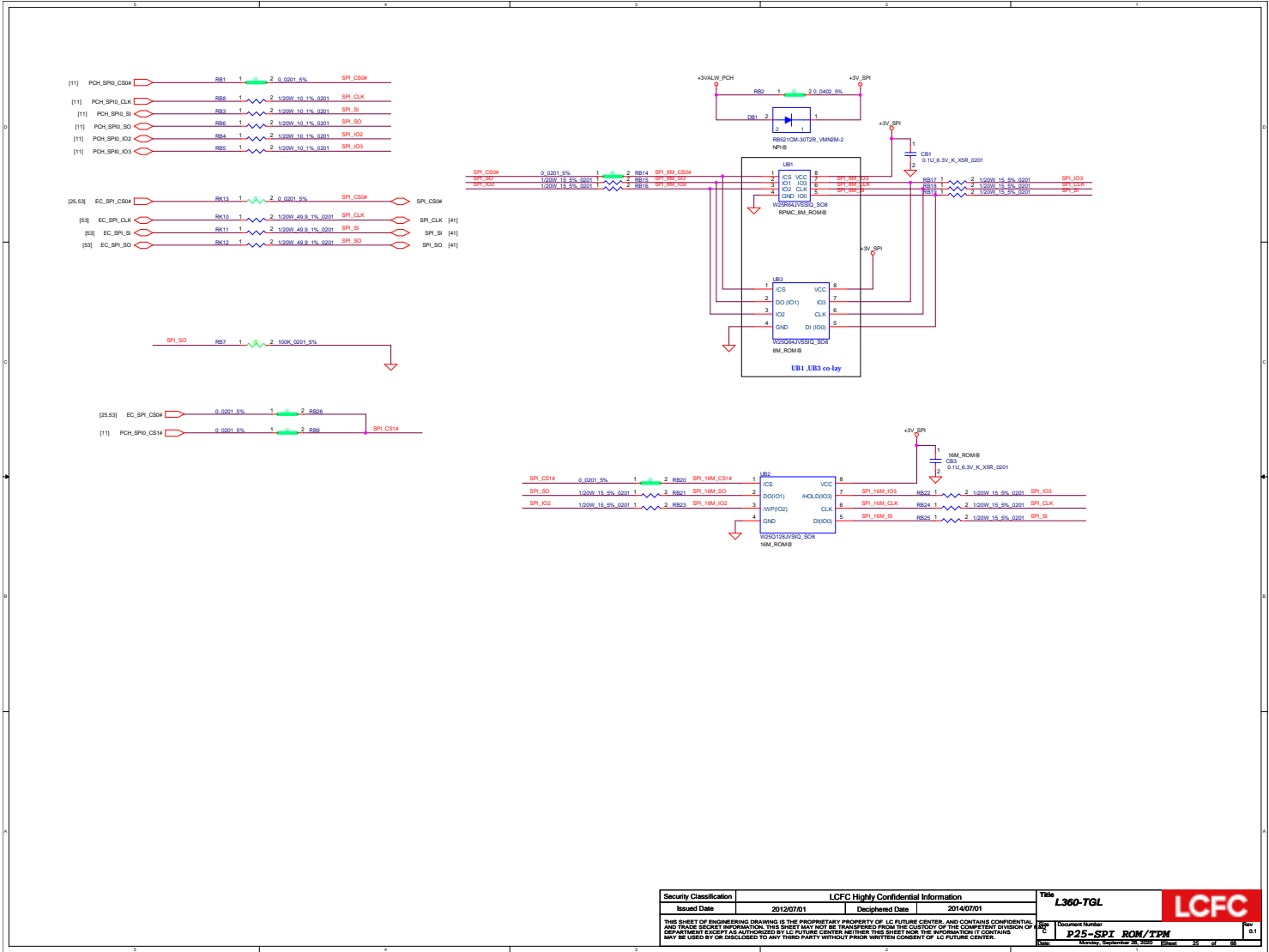
Change CFG Follow PEG VLD - Kahan 1220

Pin Name	Strap Description	Configuration	Default Value
CFG[0]	RSVD	None	
CFG[3:1]	RSVD	Pull up to VCCIO	Ikohm
CFG[4]	eFPP enable strap 1 - Disabled 0 - Enabled	Pull up to VCCIO / Pull down Platform design dependent	Ikohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training 1 - (default) PEG Train immediately following RESET# de-assertion 0 - PEG Wait for BIOS for training	Pull up to VCCIO / Pull down Platform design dependent	Ikohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull up to VCCIO	Ikohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG0 Lane Reversal 1 - Normal (default) 0 - Reversed	Pull up to VCCIO / Pull down Platform design dependent	Ikohm
CFG[17:15]	RSVD	None	

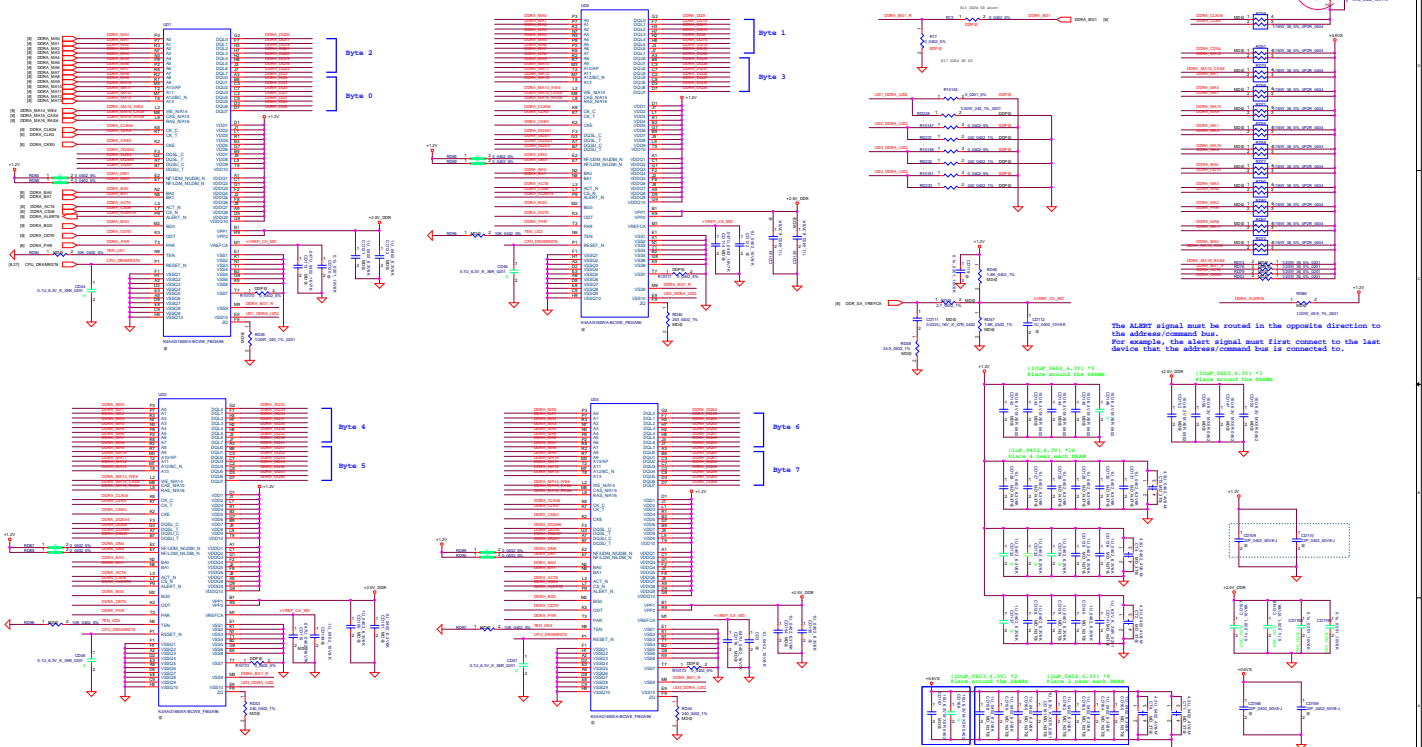
CPU PCIe Gen4 Bifurcation and Lane Reversal Mapping

Bifurcation	CFG Signals	Lanes
	CFG [14]	0 1 2 3
1x4	1	0 1 2 3
1x4(Reversed)	0	3 2 1 0

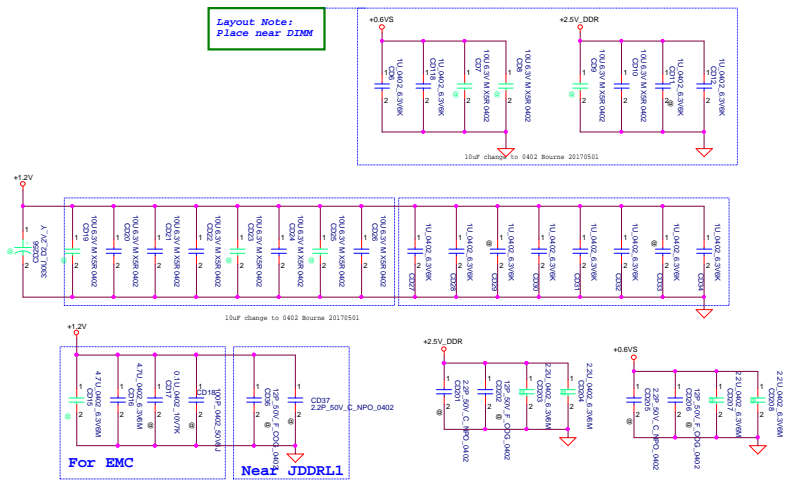
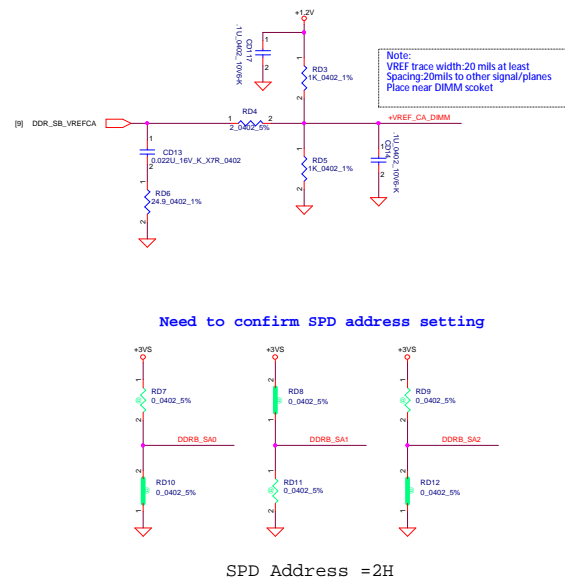
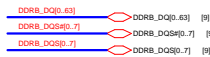
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				P23-CPU (16/16) : CFG/RESERVED
				Doc. Version: 1.0, 2009-08-25, 25, 4, 8



Apply X76 BOM to control DDP Memory Down stuff components!






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<p>Document Number: P26-D0R4 Memory Down</p>				




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Source Number			P28-VGA Notes List		
Date			Wednesday, August 12, 2008		
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			Doc Number	P29-GPU PCIe Interface	
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					P30-GPU NKM Information	0.1
				Date	Wednesday, August 13, 2008	Sheet 50 of 58


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				Date	P31-GPU +VGA Core_FSVDD	0.1
				Date	Wednesday, August 12, 2008	01 of 08

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001	P32-GPU AON/MAIN PWR/SECURITY		001	


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			Source Number	Rev	
			P34-GPU STRAP/DP/HDMI	0.1	
			Version	Sheet	
			Version 1.0	34	of 38

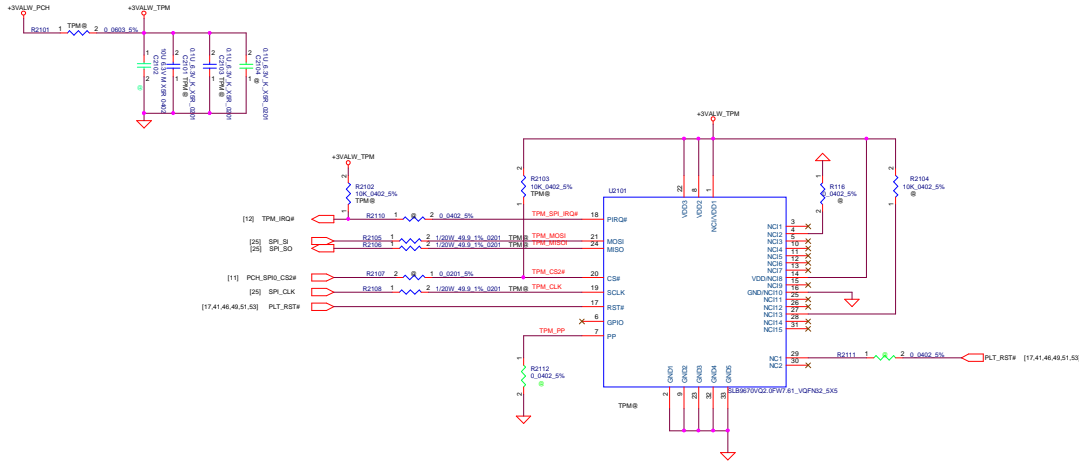
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			Doc Number	Rev	
			P35-GPU GP10/JTAG	0.1	
			Date	Wednesday, April 12, 2012	35 of 38

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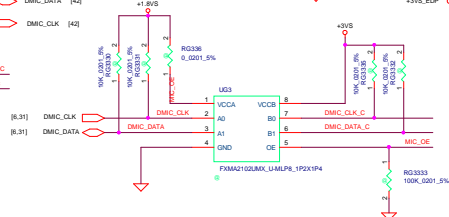
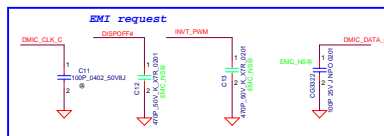
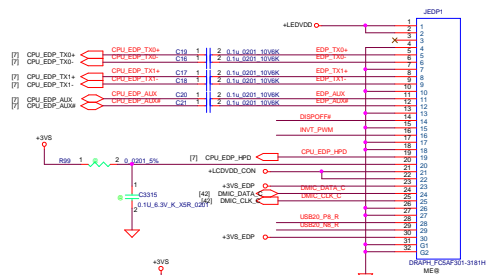
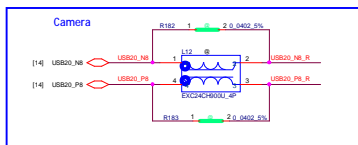
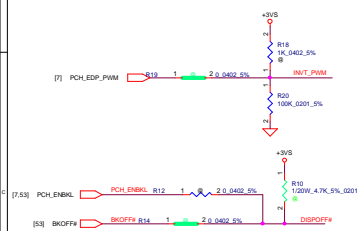
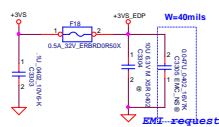
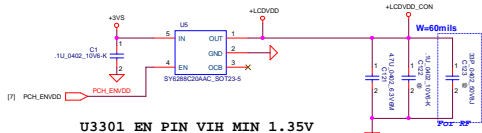
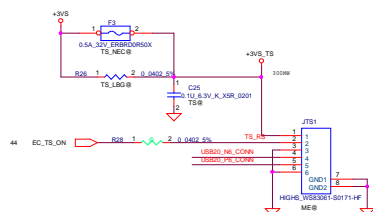
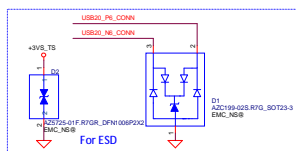
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Sheet Number		P40-BLANK		Date		Wednesday, August 17, 2011		Sheet 40 of 48	
Rev		0.1							



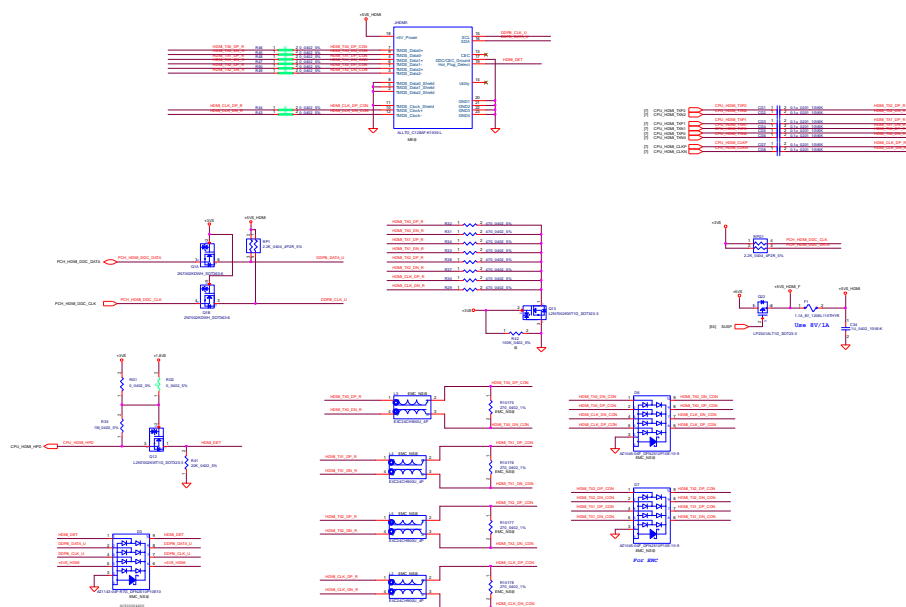
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1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	NC	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PPGPIO6	NC
5	NC	NC	NC	NC	NC
6	VNC/GPIO	GPIO	NC	GPIO3	NC
7	GPIO/VDD	PP	PP	NC	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VDD	VDD	VDD	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND

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Source Number	P41-TPM			Doc Number		Rev
Date	September 18, 2020			Sheet	41	of 61

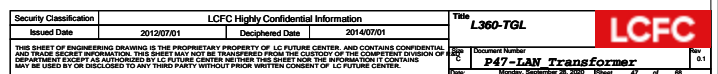
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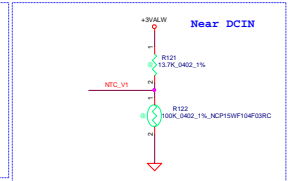
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Date		Wednesday, August 12, 2005		Sheet		44		of 88	



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REMOTE+/_R, REMOTE1+/_-, REMOTE2+/_-:  
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Trace length:<8"
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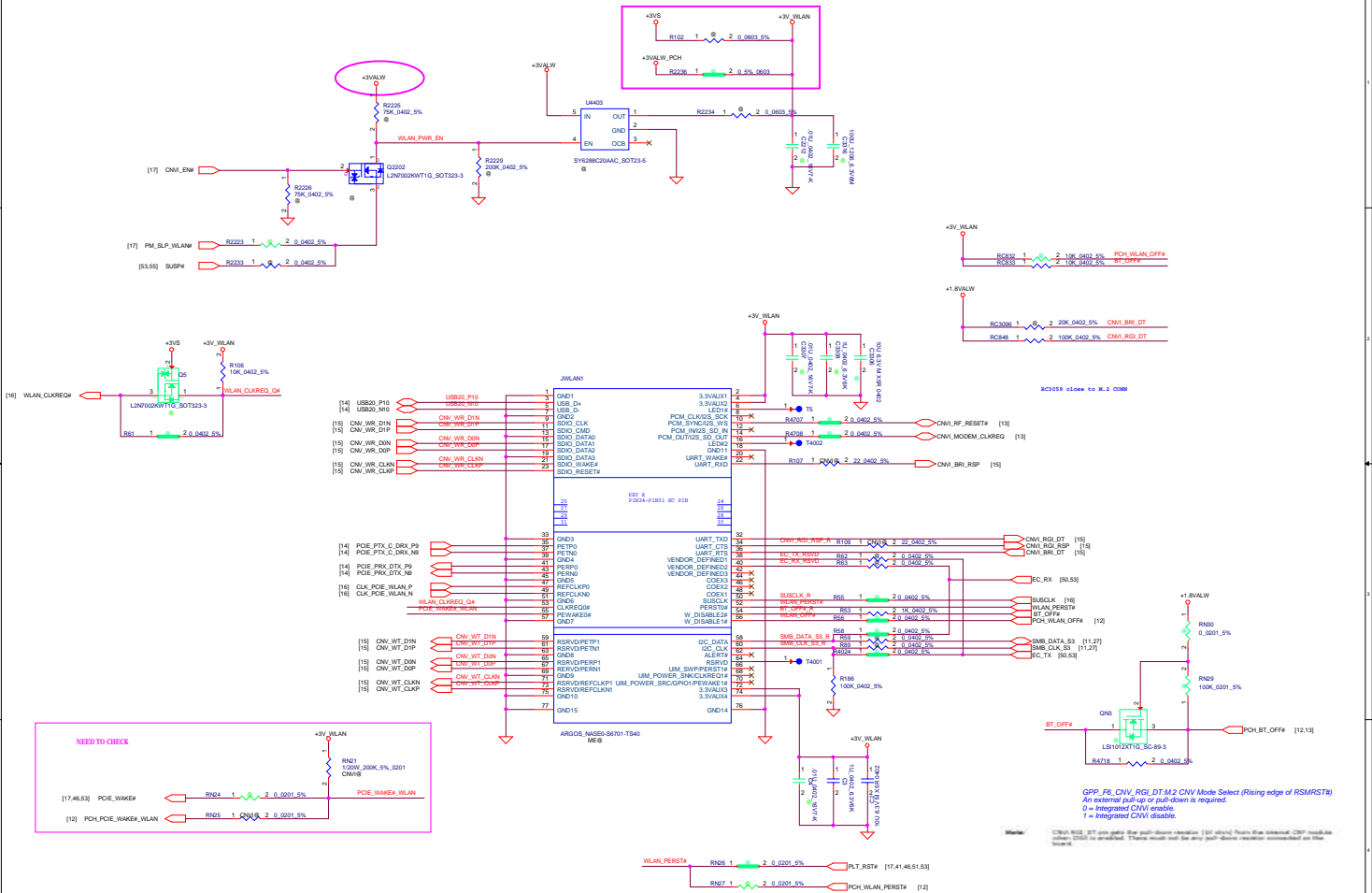


Pin connection diagram for the FAN connector. The connector is labeled "FAN Conn" and "H0GH5_WB32041-S0471-HF". The pins are numbered 1 through 6. The connections are as follows:

- Pin 1: +5V_FAN1
- Pin 2: EC_FAN_SPEED1
- Pin 3: EC_FAN_PWM1
- Pin 4: GND1
- Pin 5: GND2
- Pin 6: ME

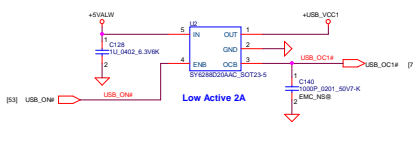
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Mini-Express Card(WLAN/WiMAX)

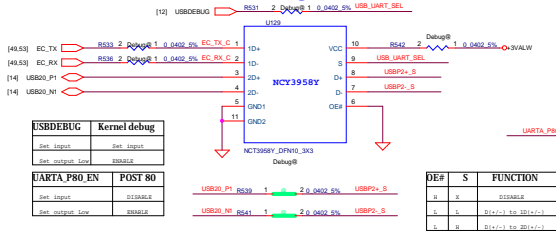


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Source Number		P49-NGFP WLAN		01	
Rev		1		01	

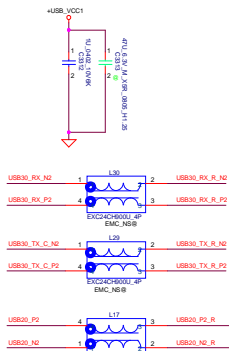
LEFT SIDE USB3.0 PORT x2



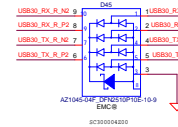
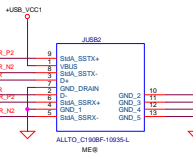
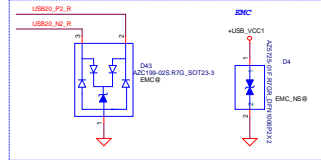
For USB Debug Function



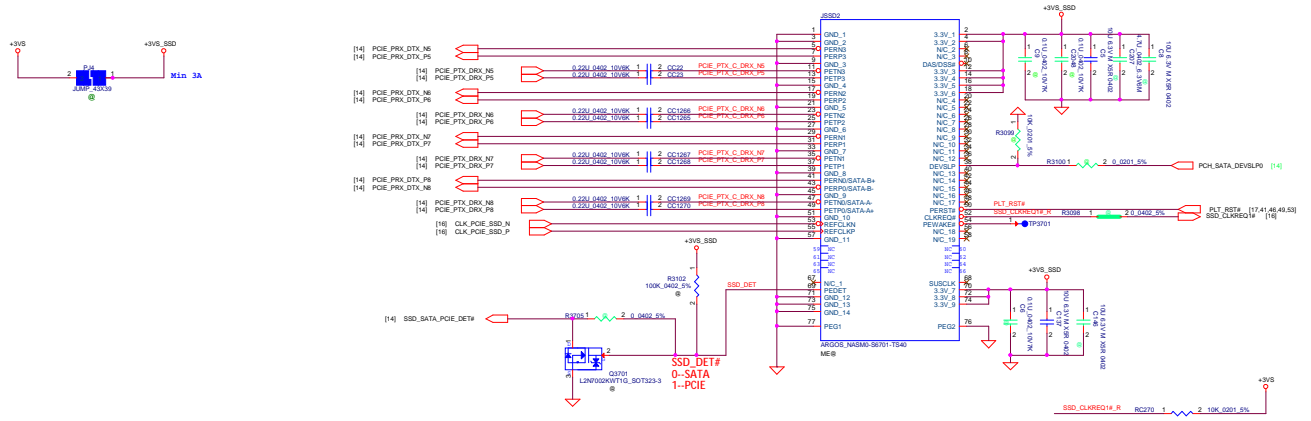
04/02 add USB debug function bron



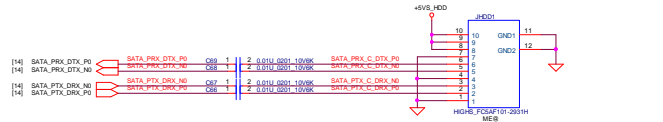
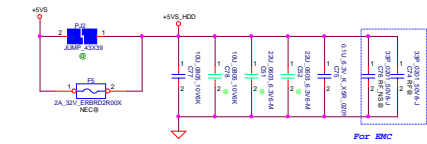
FOR ESD Close to Connector



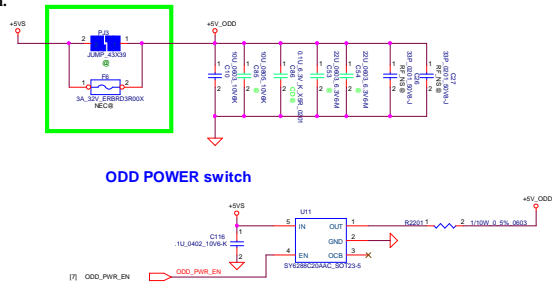
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		Rev		01	



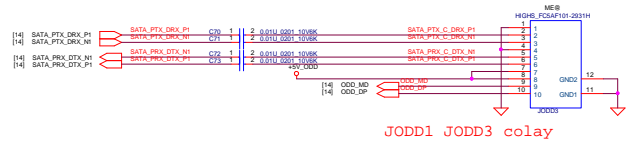
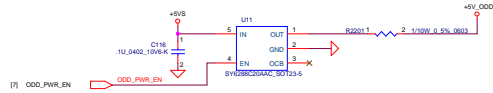
SATA HDD Conn.



ODD Conn.

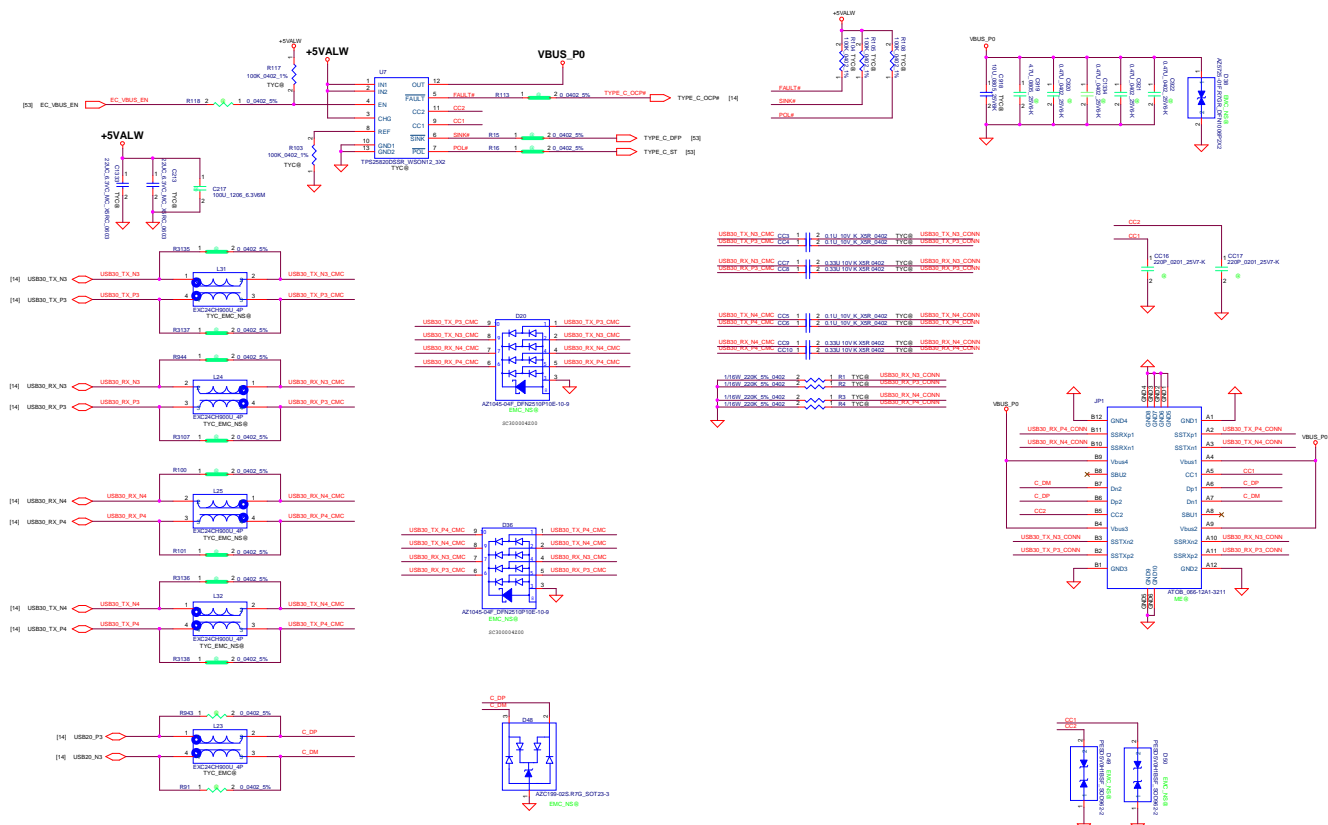


ODD POWER switch

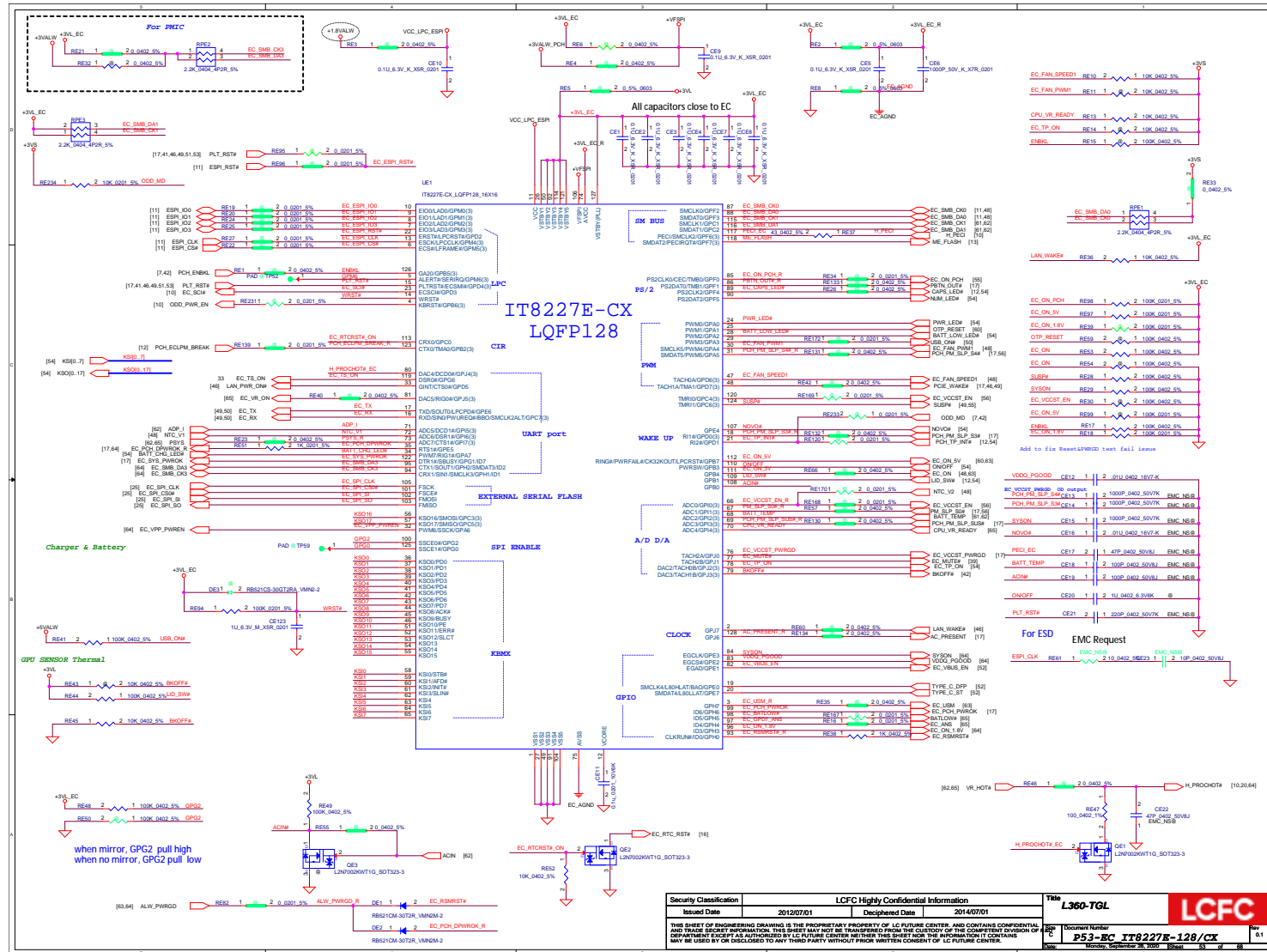


JODD1 JODD3 colay

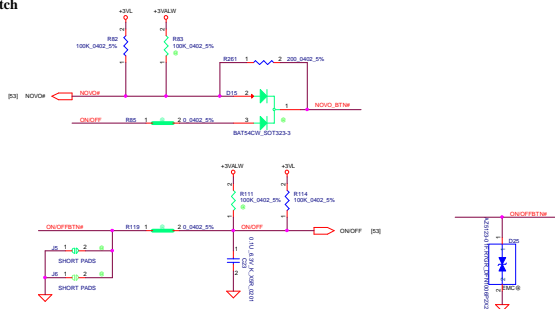
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Rev		Rev		Rev	



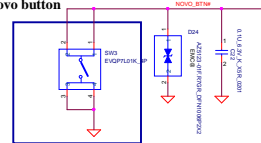
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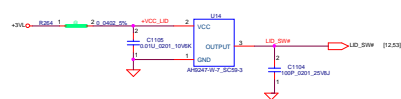
ON/OFF switch



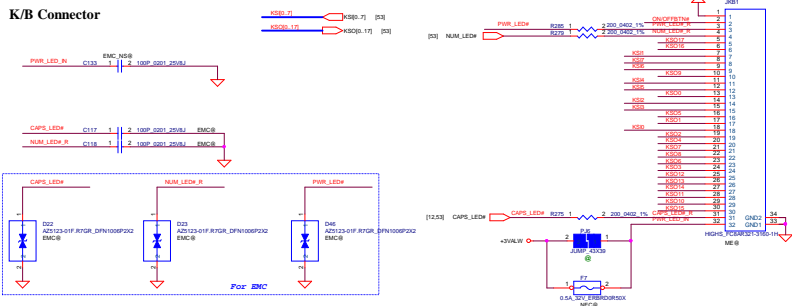
Novo button



LID switch



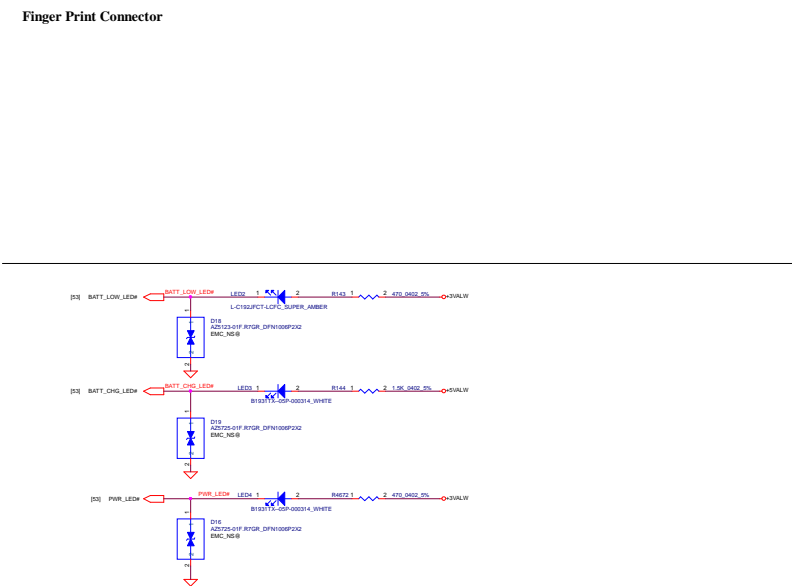
K/B Connector



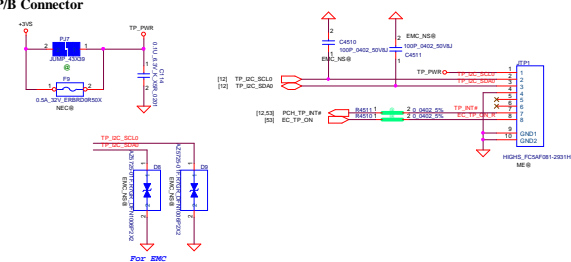
KB Backlight Connector



Finger Print Connector

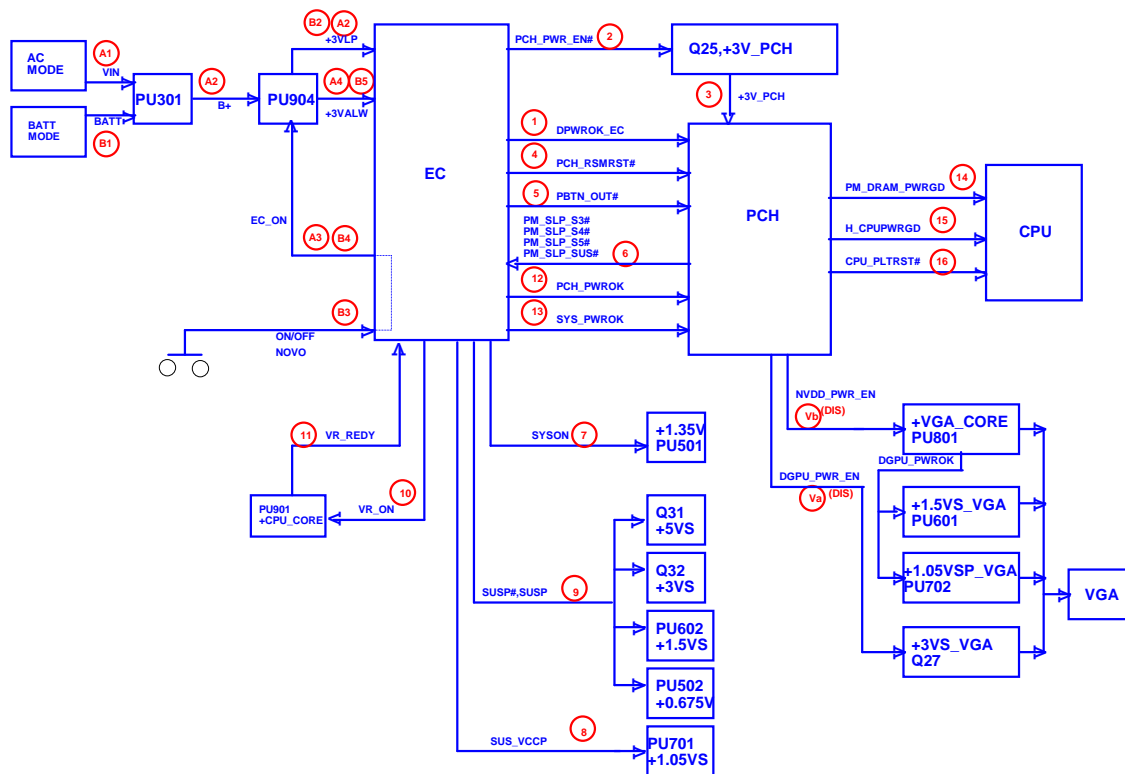


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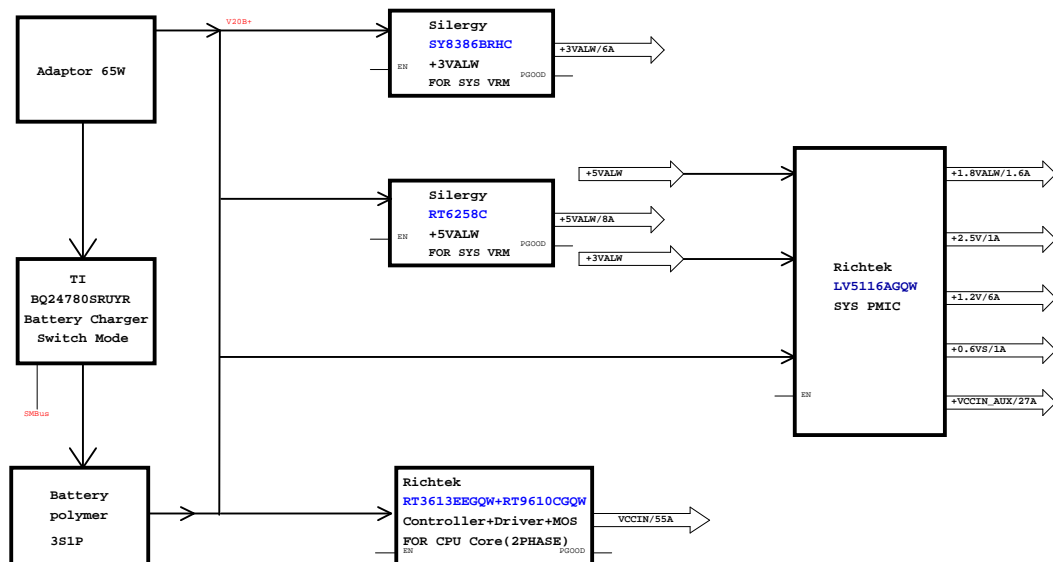


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Rev	1	Document Number	P54-KBD/PWR/LED/TP Conn.		1	

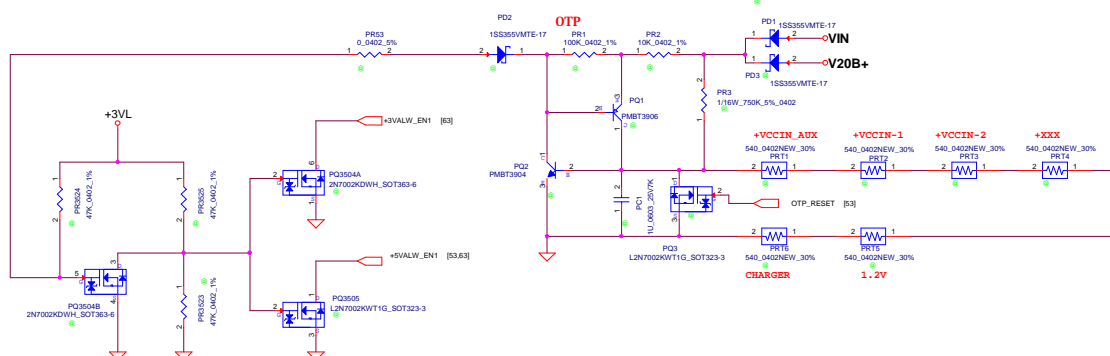





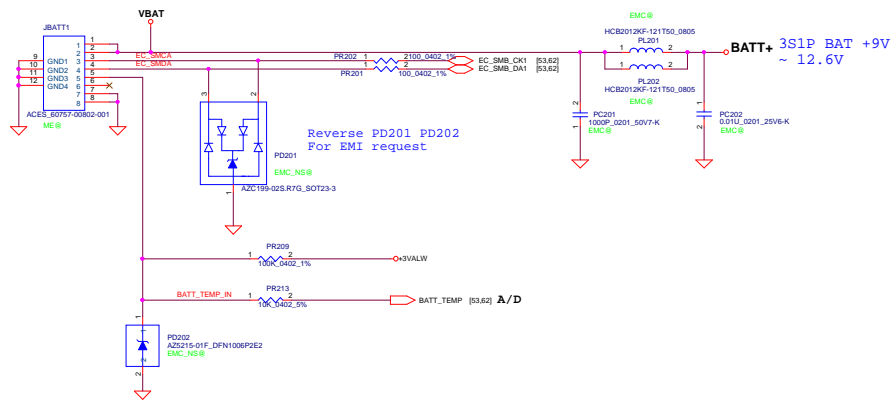
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Size	Document Number	Rev		
Custom	P57-Power Sequence Block	0.1		
Date:	Wednesday, August 15, 2012	Print	57	of 68



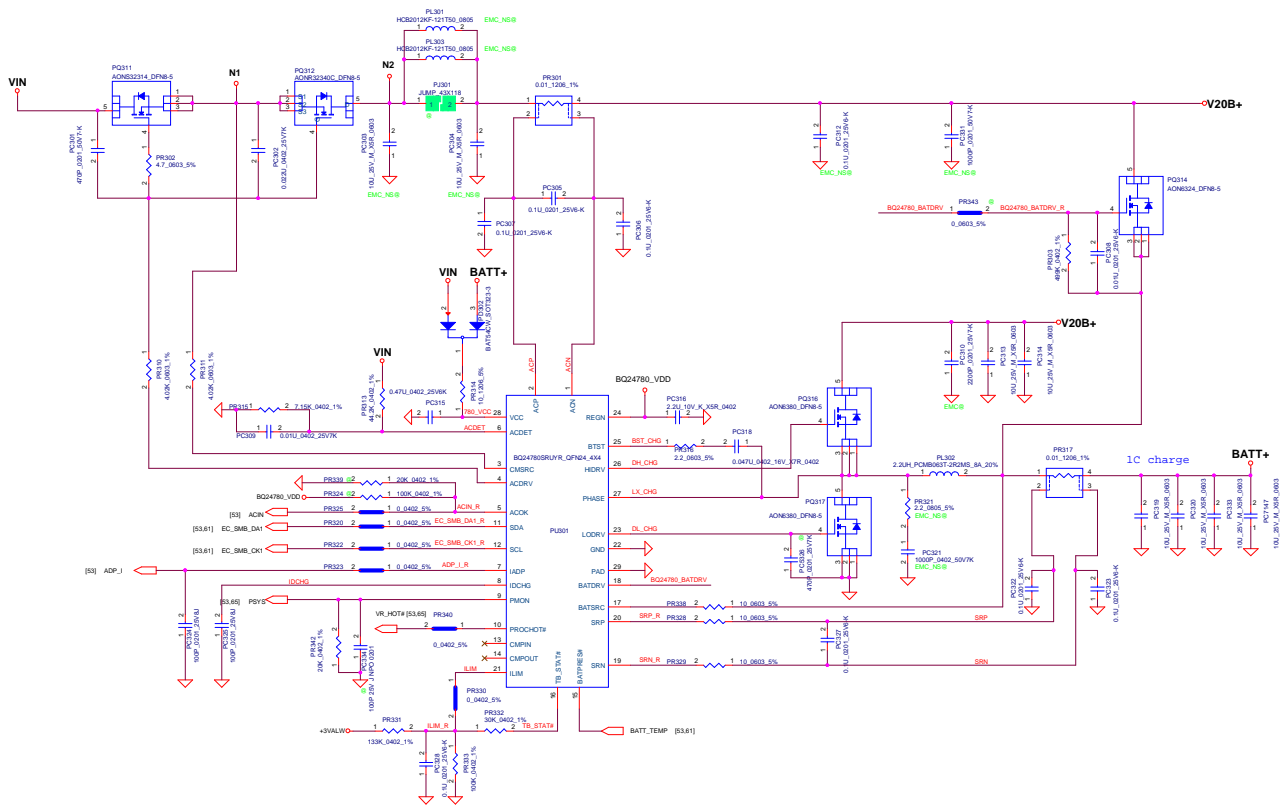
Security Classification	LC Future Center Secret Data		Title	PWR-Power Diagram	
Issued Date	2019/07/20	Designed Date	2020/07/20	Doc Number	GS55C
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Name: <small>Microelectronics R&D</small>				Page	3 of 3



Security Classification	LC Future Center Secret Data		Title	PWR-DCIN / RTC charger 	
	Issued Date	Deciphered Date	2020/07/20		
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			Date	Monday, September 28, 2020	Sheet 60 of 68

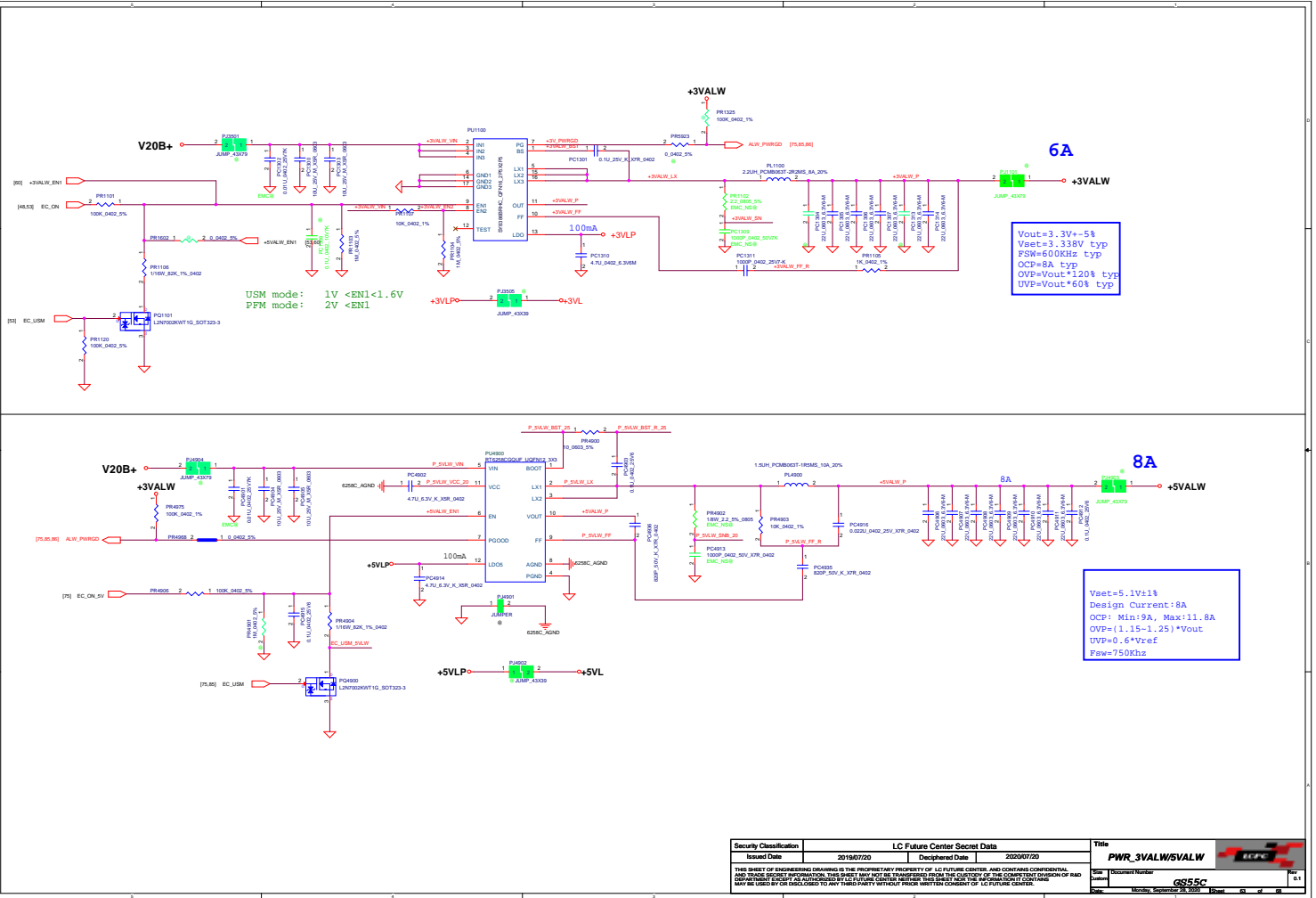


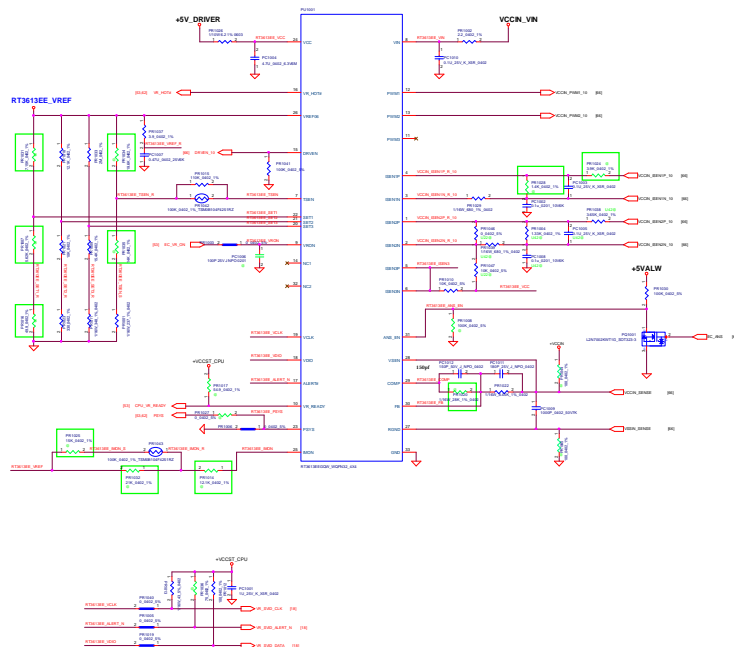
Security Classification	LC Future Center Secret Data		Title
Issued Date	2019/07/20	Deciphered Date	2020/07/20
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			Document Number GS55C
			Date: Monday, September 28, 2020 15:00:00 Sheet 61 of 68



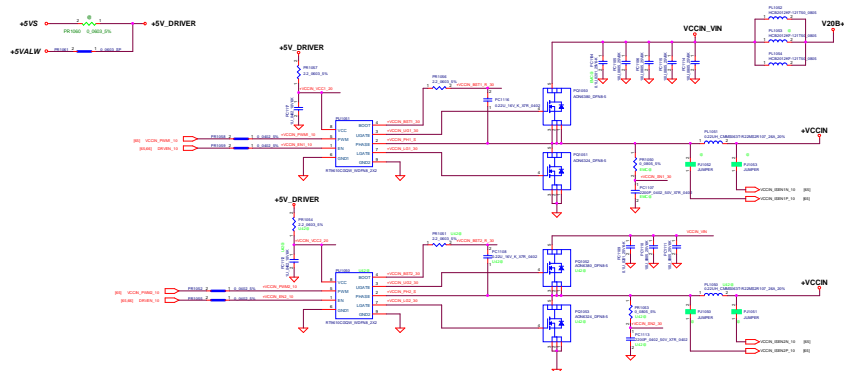
AC/DC setting 17.2V
 Charge current limit HW=7A
 DC discharge limit =26A
 Discharge current limit HW=9A during Turbo boost

Security Classification	LC Future Center Secret Data		Title	PWR-CHARGER
Issued Date	2019/07/20	Disciplined Date	2020/07/20	Document Number
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				Version
				Sheet
				25 of 28





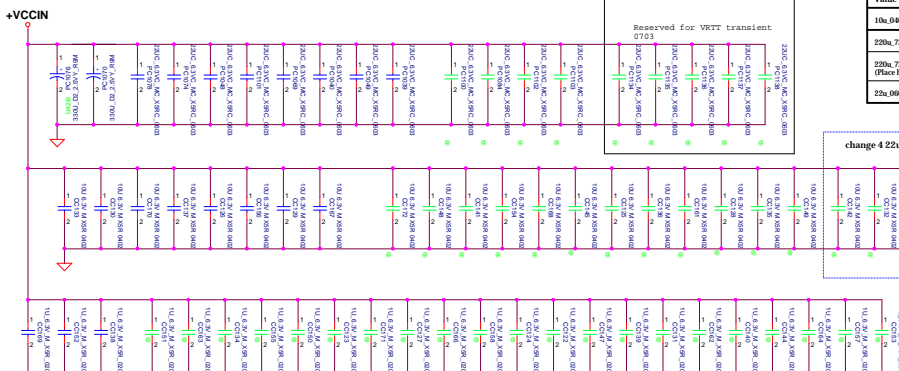
Device Classification	LCFC High-Capacitance Microcontroller	5540-701	LCFC
Manufacturer	LCFC		
Part Number	5540-701		
Package	QFN-48		
Pin Count	48		
Operating Temperature	-40°C to 125°C		
Storage Temperature	-55°C to 150°C		
Moisture Sensitivity Level (MSL)	1		
Lead (Pb) Free	Yes		
RoHS Compliant	Yes		
REMARK: This document is for reference only. The actual product specifications and pin configurations should be referred to the product datasheet.			
REMARK: The product is not recommended for use in applications requiring high reliability.			
REMARK: The product is not recommended for use in applications requiring high performance.			
REMARK: The product is not recommended for use in applications requiring high precision.			
REMARK: The product is not recommended for use in applications requiring high accuracy.			
REMARK: The product is not recommended for use in applications requiring high speed.			
REMARK: The product is not recommended for use in applications requiring high resolution.			
REMARK: The product is not recommended for use in applications requiring high precision.			
REMARK: The product is not recommended for use in applications requiring high accuracy.			
REMARK: The product is not recommended for use in applications requiring high speed.			
REMARK: The product is not recommended for use in applications requiring high resolution.			



Vboot=1.8V Loadline= 2mohm
 Ripple=30mV (0A-1A)
 Ripple=30mV (1A-5A)
 Ripple=15mV (5A-TTC)
 TDC=36A Iccmax=55A
 ICC=45A
 Max. Overshoot: 200mV/500us
 OVP=VDD+60mV
 OVP=VID-150mV
 Psw=1000 kHz

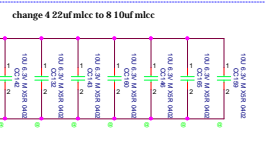
Product Classification	LCFC Highly Configurable Microsystem	5540-701	LCFC
Product Name	5540-701	5540-701	
Product Name	5540-701	5540-701	5540-701
Product Name	5540-701	5540-701	5540-701

VCCIN
 PDG: 4*220UF+ 10*22UF+12*10UF
 L360 TGL_U: 2*330UF+ 10*22UF+12*10UF+3*1UF

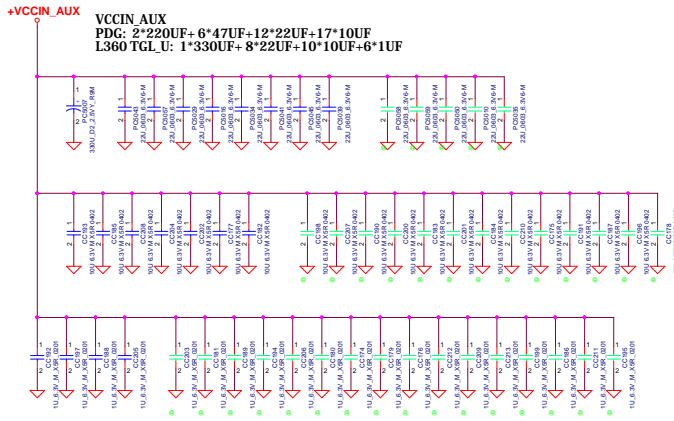


PDG: VCCIN

Value	Qty	Note
10u, 0402	12	For design change, please refer to the BOM for details.
220u, 7343	2	For design change, please refer to the BOM for details.
220u, 7343 (Flux holder)	2	For design change, please refer to the BOM for details.
22u, 0603	10	For design change, please refer to the BOM for details.



Security Classification		LCFC Highly Confidential Information		Title	S540-TGL		LCFC
Issued Date		Deciphered Date		2014/07/01			
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				Document Name	FWR CPU FWR Decoupling		



PDG: VCCIN_AUX

Value	Qty	Note
220n, 7343	2	Primary filter per 2.5V rating caps.
47u, 0805	3	MLCC capacitor recommendation based on VR solution with 150kVt VR bandwidth, 47uF 0805, switching frequency assuming 50V, 7.5A load.
47u, 0805	3	Place board caps as close as possible to package (Place holder)
22u, 0603	12	VR - 7343 - 0805 - 0603 - 0402 - package. Ripple caps along current flow path from VR to package pins.
10u, 0402	17	Secondary filter per 2.5V rating caps.
10u, 0402	10	MLCC capacitor recommendation based on VR solution with 150kVt VR bandwidth, 10uF 0402, switching frequency assuming 50V, 7.5A load. Place board caps as close as possible to package.

Security Classification	LCFC Highly Confidential Information		Title	S540-TGL	LCFC
Issued Date	2012/07/01	Declassified Date	2014/07/01		
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			Doc. Number	PWR_PCH_PWR_Decoupling	0.1
			Doc. No.	Version	Rev. 1.0
			Doc. No.	Version	Rev. 1.0